Q- AND V-BAND MMIC CHIP SET USING 0.1 μm MILLIMETER-WAVE LOW NOISE InP HEMTs

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Abstract—**A MMIC chip set for millimeter-wave (mmW) communication systems has been developed. The highlights are a 3-stage Q-band LNA with 2.0 dB NF/ 22 dB of gain and a 2-stage V-band LNA with 2.3 dB NF/ 15 dB of gain. Altogether, 7 MMIC chips (2 LNAs, 2 mixers, 2 downconverters, and 1 LO amplifier) make up this effort to develop low noise mmW building block functions in the InP HEMT technology.**

INTRODUCTION

The MMIC chip set described here represents critical components in future lightweight communication satellite applications. Not only are there considerable size and weight reductions in implementing higher levels of integration such as a downconverter MMIC chip (Figures 1 and 2), but the improved reliability from having fewer components makes the creation of MMIC building block functions highly desirable. Future satellite payloads have a need for size and weight reductions in the EHF payload without sacrificing the system performance. InP HEMTs can play a major role in meeting those needs. The InP HEMT structure (also known as AlInAs/GaInAs HEMT) has produced the lowest reported device noise figure performance at 60 GHz (about 1 dB) with 9 dB of associated gain and the highest cutoff frequency (> 300 GHz)[1]. This paper discusses the fabrication process, model development, circuit design, and measured results of 7 MMIC building block chips.

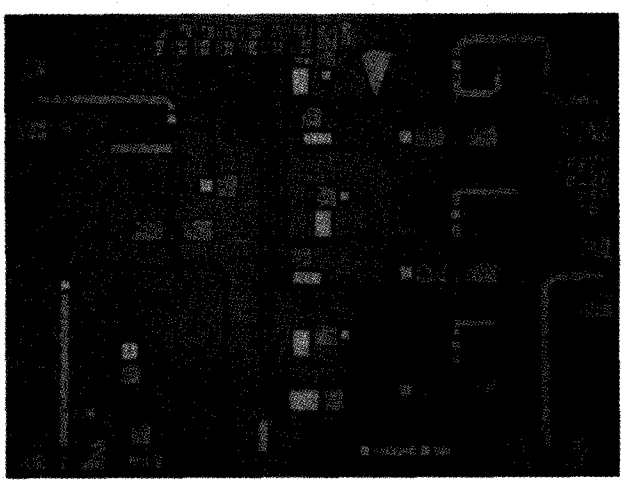

Figure 1. Q-band MMIC downconverter macro-cell layout.

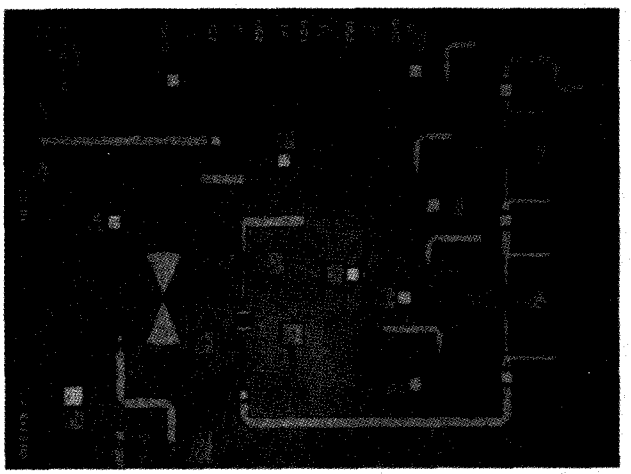

Figure 2. V-band MMIC downconverter macro-cell layout.

PROCESS DESCRIPTION

The InP HEMT structure is grown by molecular beam epitaxy (MBE) and is lattice-matched to an InP semi-insulating substrate. It consists of a 250 nm undoped AlInAs buffer with a 40 nm GaInAs channel, a 1.5 nm undoped spacer, an 8 nm AlInAs donor layer, and a 7 nm GaInAs doped cap. Electron sheet density is about 2.5 to 2.8 x 10^{12} cm^{-2} with an electron mobility between 10,000 and 11,000 cm^2/Vs at room temperature. A 100 nm silicon nitride passivation layer protects the active device from contamination and moisture but slightly degrades the performance . A novel double-exposure e-beam lithography process is used to create a highly repeatable 0.1 μm gate definition through the resist[1].

Passive components such as metal-insulator-metal (MIM) capacitors, MBE bulk resistors, microstrip transmission lines, and backside vias through a 4 mil thick substrate play an important role in MMIC design. The MIM capacitors are formed with a silicon nitride dielectric and typically have a capacitance value of 560 pF/mm^2.

DEVICE MODELS

The HEMT devices used in the designs were based on three gate widths of 50 μm, 100 μm, and 150 μm all with gate lengths of 0.1 μm and a unit finger width of 25 μm. Typical low noise bias for these devices are 7, 14, and 21 mA, respectively, with the drain at +1.0V. For high gain applications, they are biased at 10, 20, and 30 mA,

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respectively, with the drain at +1.5V. DC extrinsic transconductances are typically 560 mS/mm at the low noise bias condition and about 650 mS/mm when biased for high gain.

Obtaining noise parameters above 18 GHz through direct measurement was limited by the existing test equipment. The measurement can be made at the lower frequencies; however, achieving accurate results for ultra-low noise InP HEMTs whose noise figure is approximately 0.3 dB at 12 GHz can lead to inaccurate results when extended through Q- and V-band.

The approach that has been used here is to measure the amplifier noise figure and gain at V-and W-band and use these to predict the minimum noise figure and associated gain. The remaining noise parameters are then calculated using theoretical noise models[2,3].

Device S-parameters for Q- and V-band were generated from a 17-element HEMT model developed from measured data up to 45 GHz for use in the LNA designs. For the passive HEMT mixer designs, the Curtice Square-Law Model[4] was used to fit the I-V characteristics of the device. For the LO amplifier design, a load line analysis[5] was used to develop the output impedance of the final stage of the amplifier.

DESIGN AND RESULTS

All simulations and layouts were done using LIBRA™ and ACADEMY™ software tools on Sun SPARC work-stations. The designs were fabricated with the InP HEMT low noise process at the Hughes Research Laboratories. On-wafer S-parameter measurements were made with a CASCADE probe station and an HP 8510C or Wiltron 360

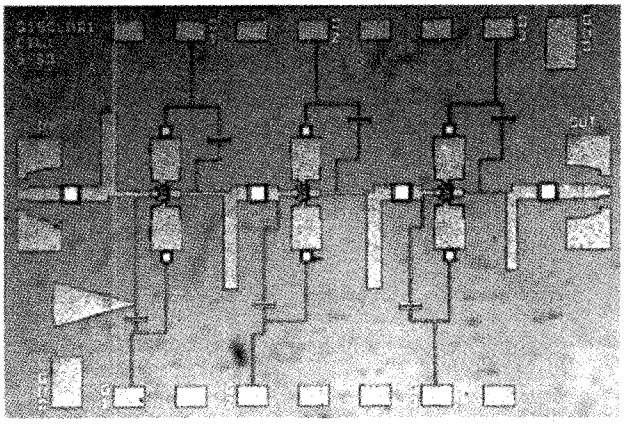

Figure 3. Three-stage Q-band MMIC LNA layout.

automatic network analyzer. Noise figure and gain measurements of the LNAs were made in a test fixture using an HP 8970B noise figure meter and have been corrected for fixture losses.

3-STAGE Q-BAND LNA

The 3-stage LNA uses three 150 µm devices each configured in a 6 x 25 µm paralliel-gate arrangement. The first stage is biased for low noise (Vds=+1.0V at 21 mA) while the other two stages are each biased for high gain (Vds=+1.5V at 30 mA). The device sizes are optimum for Q-band operation to minimize the matching network required for the best noise match[6] thereby reducing the chip size and circuit losses. Epi resistors in the gate bias

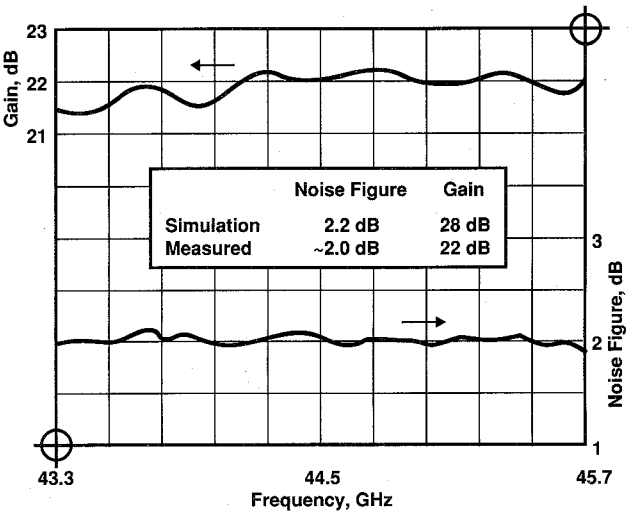

Figure 4. Noise figure and gain for the three-stage Q-band MMIC LNA.

lines provide out-of-band stability while maximizing inband gain. The chip size is 2 x 3 mm^2 (Figure 3) and consumes 111 mW of power.

The measured results show a MMIC noise figure between 1.9 and 2.1 dB with associated gain of 21.5 to 22.2 dB from 43.3 to 45.7 GHz (Figure 4). The low gain may be due to compression in several stages and is being evaluated. To our knowledge, this is the best performance ever reported for a MMIC LNA in this frequency band. Custom test fixtures were used with finline endblocks that provide waveguide to microstrip transitions.

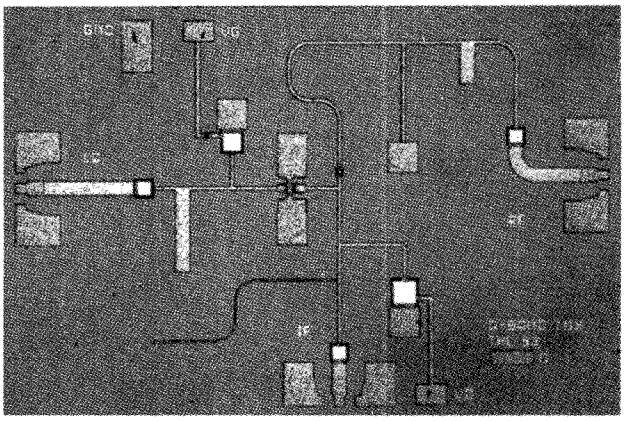

Figure 5. Q-band MMIC mixer layout.

Q-BAND MIXER

A passive HEMT downconverter mixer design was chosen for its superior intermodulation performance[7]. The design is single-ended since the isolation requirements were not demanding and the goal was to minimize the LO drive requirement and the overall chip size. The drain is biased at zero volts and the mixing function is achieved by creating a linear time varying channel resistance produced by the LO driving signal on the gate. It is this linear resistance that minimizes intermodulation products[7]. Additionally, this design features an optional drain bias line that can change the mixer into an active mixer design thereby reducing the conversion loss by 2 to 3 dB. This design uses a single

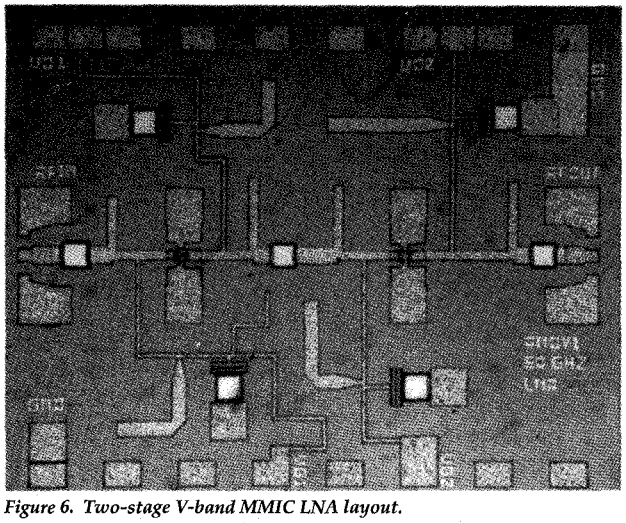

Figure 6. Two-stage V-band MMIC LNA layout.

100 µm device, 4 x 25 µm. An LO signal of +4 dBm is sufficient to drive the gate which is biased near pinch-off. The drain is designed with a bandpass diplexer network which receives the RF input signal (43.3 to 45.7 GHz) through one port, mixes with the LO frequency (26 GHz), then passes the IF frequency (17.3 to 19.7 GHz) out through the second port. The chip size is 2 x 3 mm^2 (Figure 5) and consumes negligible power when the drain is biased at zero volts.

The measured result shows a conversion loss between 9 and 11 dB for the IF frequency from 17.6 to 19.7 GHz with Vds = +0.65 V and Vgs = -0.9 V This is an improvement of 2 dB over the passive bias condition. The 2IF spur is at -44 dBc. A custom 3-port test fixture was used with a finline endblock on the RF port and K-connectors on the LO and IF ports.

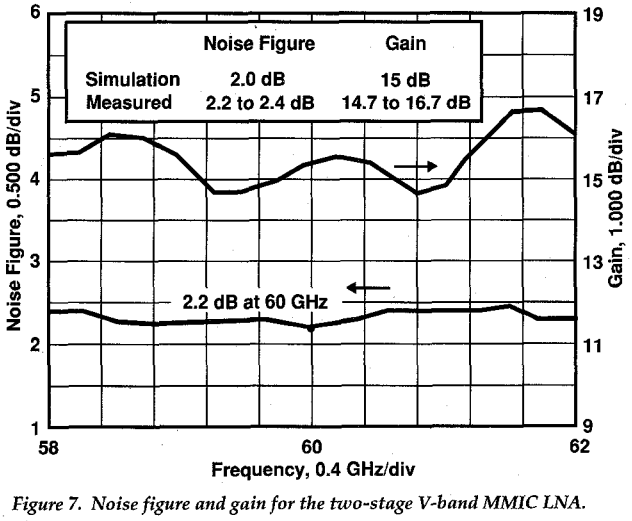

Figure 7. Noise figure and gain for the two-stage V-band MMIC LNA.

2-STAGE V-BAND LNA

The V-band LNA design uses a 100 µm device, 4 x 25 µm, biased for low noise (Vds=+1.0V at 14 mA) in the first stage and a 50 µm device biased for high gain (Vds=+1.5V at 10 mA) in the second stage. The 100 µm device was chosen to minimize the matching network required for the best noise match and return loss at V-band. The devices were stabilized with a double

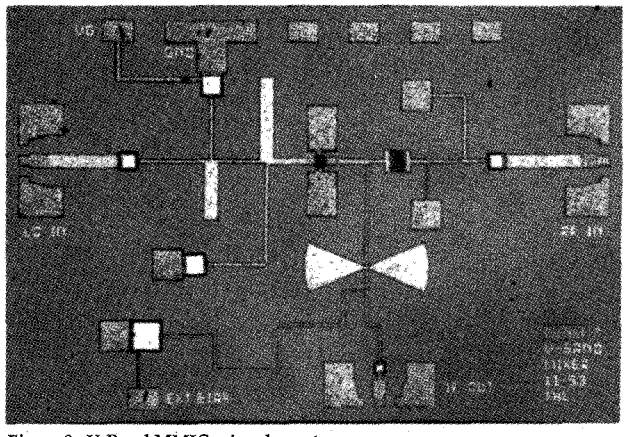

Figure 8. V-Band MMIC mixer layout.

tuned quarter-wavelength structure on the gate bias for optimum stability. Chip size is 2 x 2.5 mm^2 and consumes 29 mW of power (Figure 6).

The measured results show a noise figure between 2.2 and 2.4 dB with an associated gain of 14.7 to 16.7 dB from 58 to 62 GHz (Figure 7). To our knowledge, this is the best noise figure performance reported for a V-band MMIC and compares well to the simulation. A custom test fixture was also used that incorporated finline transitions.

V-BAND MIXER

Like the Q-band mixer, this design also uses the 100 µm device as a passive mixer and requires an LO drive signal of +4 dBm at the gate. A similar bandpass diplexer network is used on the drain of the device except that the RF frequency band is 58 to 64 GHz and the IF frequency band is 6 to 10 GHz. The optional drain bias line has also

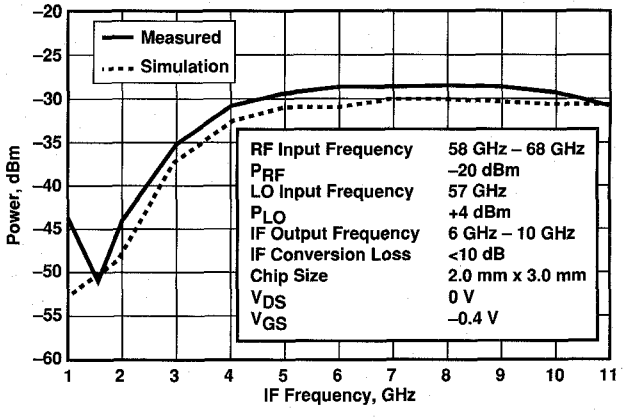

Figure 9. Response for the V-band MMIC mixer.

been incorporated into this design. The chip size is 2 x 3 mm^2 (Figure 8) and consumes negligible power.

The measured result shows a conversion loss between 8 and 10 dB for the IF frequency from 4.5 to 10.5 GHz with Vds = 0V and Vgs = -0.4 V (Figure 9) and correlates with the simulation even though the mixer was tested with an input RF frequency higher than originally designed for (this was due to limited availability of LO sources). The 2IF spur is at -32 dBc. A custom 3-port test fixture similar to the Q-band 3-port fixture was used for the measurements.

V-BAND LO AMPLIFIER

The 3-stage LO amplifier design uses a 50 µm device, 2 x 25 µm, in the first stage and a 150 µm device, 6 x 25 µm, in the second and third stages. All stages are biased for high gain with Vds=+1.5V at 10 mA for the 50 µm device and 30 mA for each of the 150 µm devices. A load line analysis was used to determine the optimum output impedance of the 150 µm device. An output

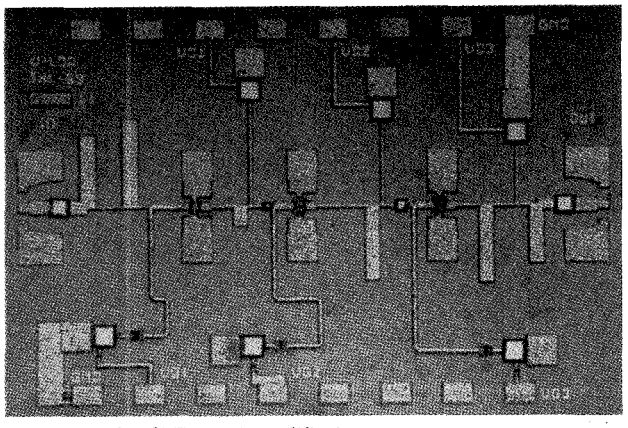

Figure 10. V-band MMIC LO amplifier layout.

matching network was then generated to maximize the power transfer during large-signal operation. The design approach then proceeded to conjugately match each preceding stage. The chip size is 2 x 3 mm^2 and consumes 105 mW of power (Figure 10).

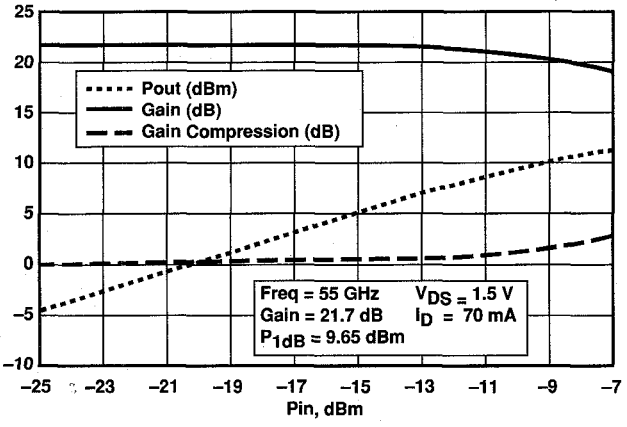

Figure 11. Response for the V-band MMIC LO amplifier.

Only limited amount of testing was performed at 55 GHz although the circuit was designed to operate from 48 to 58 GHz. Linear gain is 21.7 dB and matches the simulation. P_{1dB} is +9.65 dBm and exceeds the +8 dBm requirement (Figure 11).

MMIC DOWNCONVERTER MACRO-CELLS

The design of the Q- and V-band downconverter macro-cells were based on the individual LNA and mixer building blocks described earlier in this paper. These micro-cells were connected with 50 Ω transmission lines (Figures 1 and 2). Table 1 highlights the design goals.

Table 1. Design goals for the Q- and V-band downconverter macro-cells.

	Q-band	V-band
RF Frequency	43.5 to 45.5 GHz	58 to 64 GH
RF Power	-20 dBm	-20 dBm
LO Frequency	26 GHz	48 to 58 GHz
LO Power	+4 dBm	+4 dBm
IF Frequency	17.5 to 19.5 GHz	6 to 10 GHz
Gain	> 18 dB	> 5 dB
NF	< 2.5 dB	< 3 dB
Chip size	3 x 4 mm^2	3 x 4 mm^2

Although only a limited amount of testing has been done on the macro-cells, the initial test results are quite promising. For a micro-cell implementation of the Q-band MMIC downconverter, the results show 13 to 13.8 dB of gain and a noise figure between 1.7 and 2.4 dB when the RF is swept from 43.5 to 44.8 GHz. The results for the V-band MMIC downconverter macro-cells how between 7 and 7.5 dB of gain and a noise figure of 2.6 to 4.4 dB when the RF is swept from 61 to 62.8 GHz. More testing will be done to characterize the macro-cells completely.

SUMMARY

A MMIC chip set for mmW communication systems has been developed, resulting in an excellent, state-of-the-art 3-stage Q-band LNA with an average noise figure of 2.0 dB and 21.5 to 22.2 dB associated gain. Also reported is a 2-stage V-band LNA with an average noise figure of 2.3 dB and 14.7 to 16.7 dB associated gain. These results demonstrate the potential for ultra-low noise mmW MMIC LNAs using the advanced 0.1 µm InP HEMT process currently running at the Hughes Research Laboratories.

ACKNOWLEDGMENTS

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